# Slide Switches

# NET "SW<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;

# NET "SW<1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;

# NET "SW<2>" LOC = "H18" | IOSTANDARD = LVTTL | PULLUP ;

# NET "SW<3>" LOC = "N17" | IOSTANDARD = LVTTL | PULLUP ;

# Push-Button Switches

# NET "BTN\_EAST" LOC = "H13" | IOSTANDARD = LVTTL | PULLDOWN ;

# NET "BTN\_NORTH" LOC = "V4" | IOSTANDARD = LVTTL | PULLDOWN ;

# NET "BTN\_SOUTH" LOC = "K17" | IOSTANDARD = LVTTL | PULLDOWN ;

# NET "BTN\_WEST" LOC = "D18" | IOSTANDARD = LVTTL | PULLDOWN ;

# Rotary Push-Button Switch

# NET "ROT\_A" LOC = "K18" | IOSTANDARD = LVTTL | PULLUP ;

# NET "ROT\_B" LOC = "G18" | IOSTANDARD = LVTTL | PULLUP ;

# NET "ROT\_CENTER" LOC = "V16" | IOSTANDARD = LVTTL | PULLDOWN ;

# Eight Discrete LEDs

# NET "LED<7>" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<6>" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# NET "LED<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# Clock Sources

# NET "CLK\_50MHZ" LOC = "C9" | IOSTANDARD = LVCMOS33 ;

# NET "CLK\_SMA" LOC = "A10" | IOSTANDARD = LVCMOS33 ;

# NET "CLK\_AUX" LOC = "B8" | IOSTANDARD = LVCMOS33 ;

# PERIOD Constraint

# Define clock period for 50 MHz oscillator

# NET "CLK\_50MHZ" PERIOD = 20.0ns HIGH 40%;

# Character LCD

# NET "LCD\_E" LOC = "M18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "LCD\_RS" LOC = "L18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "LCD\_RW" LOC = "L17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# The LCD four-bit data interface is shared with the StrataFlash.

# NET "SF\_D<8>" LOC = "R15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<9>" LOC = "R16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<10>" LOC = "P17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<11>" LOC = "M15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# VGA Display Port

# NET "VGA\_RED" LOC = "H14" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;

# NET "VGA\_GREEN" LOC = "H15" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;

# NET "VGA\_BLUE" LOC = "G15" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;

# NET "VGA\_HSYNC" LOC = "F15" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;

# NET "VGA\_VSYNC" LOC = "F14" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = FAST ;

# DTE RS-232 Serial Port

# NET "RS232\_DTE\_RXD" LOC = "U8" | IOSTANDARD = LVTTL ;

# NET "RS232\_DTE\_TXD" LOC = "M13" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = SLOW ;

# DCE RS-232 Serial Port

# NET "RS232\_DCE\_RXD" LOC = "R7" | IOSTANDARD = LVTTL ;

# NET "RS232\_DCE\_TXD" LOC = "M14" | IOSTANDARD = LVTTL | DRIVE = 8 | SLEW = SLOW ;

# PS/2 Port

# NET "PS2\_CLK" LOC = "G14" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;

# NET "PS2\_DATA" LOC = "G13" | IOSTANDARD = LVCMOS33 | DRIVE = 8 | SLEW = SLOW ;

# DAC Interface

# NET "SPI\_MISO" LOC = "N10" | IOSTANDARD = LVCMOS33 ;

# NET "SPI\_MOSI" LOC = "T4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "SPI\_SCK" LOC = "U16" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "DAC\_CS" LOC = "N8" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "DAC\_CLR" LOC = "P8" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# DAC Interface

# NET "SPI\_MOSI" LOC = "T4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "AMP\_CS" LOC = "N7" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "SPI\_SCK" LOC = "U16" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "AMP\_SHDN" LOC = "P7" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "AMP\_DOUT" LOC = "E18" | IOSTANDARD = LVCMOS33 ;

# ADC Interface

# NET "AD\_CONV" LOC = "P11" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "SPI\_SCK" LOC = "U16" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "SPI\_MISO" LOC = "N10" | IOSTANDARD = LVCMOS33 ;

# StrataFlash Address Inputs

# NET "SF\_A<24>" LOC = "A11" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<23>" LOC = "N11" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<22>" LOC = "V12" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<21>" LOC = "V13" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<20>" LOC = "T12" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<19>" LOC = "V15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<18>" LOC = "U15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<17>" LOC = "T16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<16>" LOC = "U18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<15>" LOC = "T17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<14>" LOC = "R18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<13>" LOC = "T18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<12>" LOC = "L16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<11>" LOC = "L15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<10>" LOC = "K13" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<9>" LOC = "K12" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<8>" LOC = "K15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<7>" LOC = "K14" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<6>" LOC = "J17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<5>" LOC = "J16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<4>" LOC = "J15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<3>" LOC = "J14" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<2>" LOC = "J12" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<1>" LOC = "J13" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<0>" LOC = "H17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# StrataFlash Data I/Os

# NET "SF\_D<15>" LOC = "T8" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<14>" LOC = "R8" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<13>" LOC = "P6" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<12>" LOC = "M16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<11>" LOC = "M15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<10>" LOC = "P17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<9>" LOC = "R16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<8>" LOC = "R15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<7>" LOC = "N9" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<6>" LOC = "M9" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<5>" LOC = "R9" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<4>" LOC = "U9" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<3>" LOC = "V9" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<2>" LOC = "R10" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_D<1>" LOC = "P10" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SPI\_MISO" LOC = "N10" | IOSTANDARD = LVCMOS33 | DRIVE = 6 | SLEW = SLOW ;

# StrataFlash Control Pins

# NET "SF\_BYTE" LOC = "C17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_CE0" LOC = "D16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_OE" LOC = "C18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_STS" LOC = "B18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_WE" LOC = "D17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# SPI Flash Connections

# # some connections shared with SPI Flash, DAC, ADC, and AMP

# NET "SPI\_MISO" LOC = "N10" | IOSTANDARD = LVCMOS33 ;

# NET "SPI\_MOSI" LOC = "T4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "SPI\_SCK" LOC = "U16" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "SPI\_SS\_B" LOC = "U3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# NET "SPI\_ALT\_CS\_JP11" LOC = "R12" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 6 ;

# DDR SDRAM Address Inputs

# NET "SD\_A<12>" LOC = "P2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<11>" LOC = "N5" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<10>" LOC = "T2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<9>" LOC = "N4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<8>" LOC = "H2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<7>" LOC = "H1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<6>" LOC = "H3" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<5>" LOC = "H4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<4>" LOC = "F4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<3>" LOC = "P1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<2>" LOC = "R2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<1>" LOC = "R3" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_A<0>" LOC = "T1" | IOSTANDARD = SSTL2\_I ;

# DDR SDRAM Data I/Os

# NET "SD\_DQ<15>" LOC = "H5" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<14>" LOC = "H6" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<13>" LOC = "G5" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<12>" LOC = "G6" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<11>" LOC = "F2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<10>" LOC = "F1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<9>" LOC = "E1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<8>" LOC = "E2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<7>" LOC = "M6" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<6>" LOC = "M5" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<5>" LOC = "M4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<4>" LOC = "M3" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<3>" LOC = "L4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<2>" LOC = "L3" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<1>" LOC = "L1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_DQ<0>" LOC = "L2" | IOSTANDARD = SSTL2\_I ;

# DDR SDRAM Control Pins

# NET "SD\_BA<0>" LOC = "K5" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_BA<1>" LOC = "K6" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_CAS" LOC = "C2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_CK\_N" LOC = "J4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_CK\_P" LOC = "J5" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_CKE" LOC = "K3" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_CS" LOC = "K4" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_LDM" LOC = "J2" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_LDQS" LOC = "L6" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_RAS" LOC = "C1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_UDM" LOC = "J1" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_UDQS" LOC = "G3" | IOSTANDARD = SSTL2\_I ;

# NET "SD\_WE" LOC = "D1" | IOSTANDARD = SSTL2\_I ;

# # Path to allow connection to top DCM connection

# NET "SD\_CK\_FB" LOC = "B9" | IOSTANDARD = LVCMOS33 ;

# Prohibit VREF pins

# CONFIG PROHIBIT = D2;

# CONFIG PROHIBIT = G4;

# CONFIG PROHIBIT = J6;

# CONFIG PROHIBIT = L5;

# CONFIG PROHIBIT = R4;

# 10/100 Ethernet PHY Inputs

# NET "E\_COL" LOC = "U6" | IOSTANDARD = LVCMOS33 ;

# NET "E\_CRS" LOC = "U13" | IOSTANDARD = LVCMOS33 ;

# NET "E\_MDC" LOC = "P9" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_MDIO" LOC = "U5" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_RX\_CLK" LOC = "V3" | IOSTANDARD = LVCMOS33 ;

# NET "E\_RX\_DV" LOC = "V2" | IOSTANDARD = LVCMOS33 ;

# NET "E\_RXD<0>" LOC = "V8" | IOSTANDARD = LVCMOS33 ;

# NET "E\_RXD<1>" LOC = "T11" | IOSTANDARD = LVCMOS33 ;

# NET "E\_RXD<2>" LOC = "U11" | IOSTANDARD = LVCMOS33 ;

# NET "E\_RXD<3>" LOC = "V14" | IOSTANDARD = LVCMOS33 ;

# NET "E\_RXD<4>" LOC = "U14" | IOSTANDARD = LVCMOS33 ;

# NET "E\_TX\_CLK" LOC = "T7" | IOSTANDARD = LVCMOS33 ;

# NET "E\_TX\_EN" LOC = "P15" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_TXD<0>" LOC = "R11" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_TXD<1>" LOC = "T15" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_TXD<2>" LOC = "R5" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_TXD<3>" LOC = "T5" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# NET "E\_TXD<4>" LOC = "R6" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

# Accessory Headers

# ==== FX2 Connector (FX2) ====

# NET "FX2\_CLKIN" LOC = "E10" | IOSTANDARD = LVCMOS33 ;

# NET "FX2\_CLKIO" LOC = "D9" | IOSTANDARD = LVCMOS33 | SLEW = FAST | DRIVE = 8 ;

# NET "FX2\_CLKOUT" LOC = "D10" | IOSTANDARD = LVCMOS33 | SLEW = FAST | DRIVE = 8 ;

# NET "FX2\_IO<1>" LOC = "B4" | IOSTANDARD = LVCMOS33 | SLEW = FAST | DRIVE = 8 ;

# NET "FX2\_IO<2>" LOC = "A4" | IOSTANDARD = LVCMOS33 | SLEW = FAST | DRIVE = 8 ;

# NET "FX2\_IO<3>" LOC = "D5" | IOSTANDARD = LVCMOS33 | SLEW = FAST | DRIVE = 8 ;

# NET "FX2\_IO<4>" LOC = "C5" | IOSTANDARD = LVCMOS33 | SLEW = FAST | DRIVE = 8 ;

# FPGA Connections to CPLD

# NET "XC\_CMD<1>" LOC = "N18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "XC\_CMD<0>" LOC = "P18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "XC\_D<2>" LOC = "F17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "XC\_D<1>" LOC = "F18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "XC\_D<0>" LOC = "G16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "FPGA\_M2" LOC = "T10" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "FPGA\_M1" LOC = "V11" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "FPGA\_M0" LOC = "M10" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "XC\_CPLD\_EN" LOC = "B10" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "XC\_TRIG" LOC = "R17" | IOSTANDARD = LVCMOS33 ;

# NET "XC\_GCK0" LOC = "H16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "GCLK10" LOC = "C9" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SPI\_SCK" LOC = "U16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# SF\_A<24> is the same as FX2\_IO<32>

# NET "SF\_A<24>" LOC = "A11" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<23>" LOC = "N11" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<22>" LOC = "V12" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<21>" LOC = "V13" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# NET "SF\_A<20>" LOC = "T12" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# XC2C64A CPLD

# NET "XC\_WDT\_EN" LOC = "P16" | IOSTANDARD = LVCMOS33 ;

# NET "XC\_CMD<1>" LOC = "P30" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_CMD<0>" LOC = "P29" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_D<2>" LOC = "P36" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_D<1>" LOC = "P34" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_D<0>" LOC = "P33" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "FPGA\_M2" LOC = "P8" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "FPGA\_M1" LOC = "P6" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "FPGA\_M0" LOC = "P5" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_CPLD\_EN" LOC = "P42" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_TRIG" LOC = "P41" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_DONE" LOC = "P40" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_PROG\_B" LOC = "P39" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "XC\_GCK0" LOC = "P43" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "GCLK10" LOC = "P1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "SPI\_SCK" LOC = "P44" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# SF\_A<24> is the same as FX2\_IO<32>

# NET "SF\_A<24>" LOC = "P23" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "SF\_A<23>" LOC = "P22" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "SF\_A<22>" LOC = "P21" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "SF\_A<21>" LOC = "P20" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;

# NET "SF\_A<20>" LOC = "P19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW ;